REMARKS

Claims 1-26 were originally pending in this application. On June 22, 2005, Applicant responded to a restriction requirement by electing to withdraw claims 11, 12, and 20-26. Claims 1-10 and 13-19 are currently pending. The Office has objected to claims 1-10 and 13-19 under 35 USC § 103(a) as being unpatentable over Asahi (U.S. Pat. No. 6,975,516) in view of Blakely et al. (U.S. Pat. No. 6,618,266). This Office action was made final and is responsive to Applicant's communication filed on or about October 28, 2005. This reply is being filed with a request for continued examination.

Amendments to the Claims 1 and 13

Applicant asks that the amendments to the claims be entered into this application. Support for the amendments is found in the specification and drawings, for example Figure 2 of the drawings and paragraph 24 of the specification. No new subject matter is being added.

103(a) Rejection of Independent Claims 1 and 13

The prior art of record does not show or suggest "an embedded discrete surface mount first decoupling capacitor mounted to the outer surface of the first reference plane layer" or "an embedded discrete surface mount second decoupling capacitor mounted to the outer surface of the second reference plane layer," as required by Applicant. The Office concedes that Asahi "does not explicitly disclose the first capacitor mounted to a surface of the first reference plane layer and the second capacitor is mounted to surface of a second reference plane layer." (Page 2, end of second paragraph in section 2.) Asahi also fails to show or suggest that the capacitors are mounted on the outer surface of the reference plane layers as now required by Applicant.

The Office combined Blakely with Asahi and asserts that Blakely discloses "a first decoupling capacitor (104a) mounted to a surface of the first reference plane layer (102c)" and further references figures 3-6. (Page 2, third paragraph of section 2.) Applicant disagrees. Blakely clearly teaches a four layer printed circuit board (PCB) as shown in figure 6. The PCB has four layers referenced as 102a, 102b, 102c, and 102d.

Layers 102a and 102b are signal layers and 102c and 102d are reference or power layers. Blakely clearly states "FIG. 6 is a side view of the PCB 102 with a single power plane 102c and a single ground plane 102d." (Col. 4, lines 33-35.) Blakely further states that "four capacitors 104a, 104b, 104c, and 104d are mounted on the PCB 102, two 104a, 104b on the top layer 102a and two 104c, 104d on the bottom layer 102b of the PCB 102." (Col. 3, lines 50-53.) It is clear from Blakely's own teaching that the capacitors are mounted not on the reference or power planes 102c, 102d as required by Applicant but instead on the signal layers 102a and 102b. At least these elements, required by Applicant, are missing from the prior art references. Therefore, the rejection is improper and the claims are allowable over the prior art made of record.

103(a) Rejection of the Dependent Claims

Claims depending from claims 1 and 13 are allowable for at least the same reasons presented above.

CONCLUSION

Applicant asks that the Office reconsider this application and allow all pending claims. Please charge any fees that might be due, excluding the issue fee, to deposit account 14-0225.

Respectfully submitted,

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